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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/851,943	05/10/2001	Yasuyuki Mishima	HITA.0053	4052

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EXAMINER	
KOVALICK, VINCENT E	
ART UNIT	**PAPER NUMBER**
2673	10

DATE MAILED: 06/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/851,943	MISHIMA ET AL.	
	Examiner	Art Unit	
	Vincent E Kovalick	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to Applicant's "Response to Amendment" dated May 18, 2004 in response to USPTO Office Action dated February 19, 2004.

Applicant's Remarks have been reviewed and center on the issue that there is a common Assignee (Hitachi, Ltd.) in both the application under consideration and the primary prior art (Yamashita et al., USP 6,320,630) that was used in the rejection of each of the claims included in the final rejection. Because of the common Assignee issue, the Yamashita et al. prior art is not valid and the final rejection dated February 19, 2004 is herewith withdrawn.

In that applicant's remarks are based on the Yamashita et al. patent being invalid prior art, and the new action set forth hereinbelow is based on other prior art, Applicant's remarks relative to claims 1-17 are rendered moot.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1-2, 4-5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ode et al. (US 2001/0024183) taken with Kawamoto et al. (USP 6,023,310).

Relative to claim 1, Ode et al. **teaches** a Liquid Crystal Display (LCD) device (pg. 1 paras. 0014-0019 and pg. 2, paras. 0020-0025); Ode et al. further **teaches** a display device comprising a

liquid crystal display element and a plural driving circuits; a display control device which transmits display data and a clock signal to the plurality driving circuits (pg. 3, paras. 0049-0051; paras. 0059-0069 and Figs. 1 and 2); and a circuit board which is provided between the display control device and the plural driving circuits and supplies the display data and the clock signal transmitted from the display control device, to each of the driving circuits via a bus line and a clock line in the circuit board (paras. 0176-0180, Figs. 19 A & B and Fig. 20); further, Ode et al. **teaches** at least one of the bus line and the clock signal line of the circuit board being formed in a continuous area along a long side direction of the circuit board (pg. 3, para. 0064);

It being understood that the placement of the bus lines and clock signal lines could be located along a long side direction of the circuit board; per case law (To shift location of parts; In re Japikse, 86 USPQ 70 (CCPA 1950)).

Ode. et al. **does not teach** at least one bus line being divided into plural lines along the long side direction, and said divided plural lines are connected to the display control device individually .

Ode et al. teaches a video signal line driving circuit of a LCD for the purpose of enabling multilevel gradation display.

Kawamoto et al. **teaches** an active matrix LCD with repeating line patterns (col. 3, lines 23-57 and Fig. 1A); Kawamoto et al. further **teaches** at least one bus line being divided into plural lines along the long side direction, and said divided plural lines are connected to the display control device individually (col. 2, lines 60-66 and Fig. 1A).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the devices as taught by Ode et al. the features as taught by Kawamoto et al. in order to put in place a circuit board on which the connecting bus lines and signal lines are

accommodated to make the connection between the display control driver and associated data, clock and control line drive circuits.

Regarding claims 2 and 5, Ode et al. further **teaches** a said display device wherein the display control device supplies the display data and the clock signal to each of the divided bus lines and clock signal lines in sequence in accordance with transmission timing (pg. 3, para. 0063). It being understood that with the teaching of Ode et al. wherein the display control device generates all the signals to drive the image display device, the said display control device would generate the data and clock signals to each of the divided bus lines and clock signal lines in sequence in accordance with transmission timing.

Regarding claim 4, it being understood that with the means to divide bus lines and clock signal lines (as taught by Kawamoto et al.), the division could be limited to just two lines.

As to claim 8, Ode et al. **teaches** said display device wherein the clock signal is a clock signal for latching display data (pg. 3, para. 0065).

4. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ode et al. taken with Kawamoto et al as applied to claim 2 and 5 respectively in item 3 hereinabove, and further in view of Hamilton et al. (USP 4,503,494).

Regarding claims 3 and 6, Ode et al. **does not teach** said display device wherein the display control device supplies a signal of fixed voltage level to each of the divided bus lines and clock signal lines to which the display data and the clock signal are not supplied.

Ode et al. teaches a video signal line driving circuit of a LCD for the purpose of enabling multilevel gradation display.

Hamilton et al. **teaches** a display control circuit which generates a fixed voltage for application

to system bus lines (col. 28, lines 32-67 and col. 29, lines 1-63); Hamilton et al. further **teaches** a control circuit generating a fixed voltage for application to system bus lines wherein a fixed voltage is supplied to a bus line when a data/clock signal is not supplied (col. 29, lines 28-44). It being understood that the system bus lines are brought to a fixed voltage state independent of whether the bus lines are for transmitting date of clock signal.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Ode et al. taken with Kawamoto et al. the feature as taught by Hamilton et al. in order to eliminate the condition whereby the voltage on the bus line would be left floating.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ode et al. taken with Kawamoto et al. as applied to claim 4 in item 3 hereinabove, and further in view of Chiba et al. (USP 6,380,918).

Regarding claim 7, Ode et al. taken with Kawamoto et al. **does not teach** said display device wherein a connector for mounting the display data and the clock signal from the display control device is provided in a lengthwise central portion of the circuit board.

Ode et al. taken with Kawamoto et al. teaches a video signal line driving circuit of a LCD for the purpose of enabling multilevel gradation display wherein signal lines are divided to accommodate the distribution of signals that have multiple applications in the same system.

Chiba et al. **teaches** a display device (col. 2, lines 16-67; col. 4, lines 1-67; col. 5, lines 1-36 and Fig. 1); Chiba et al. further **teaches** a display device wherein a connector for inputting the display data and the clock signal from the display control device is provided in a lengthwise central portion of the circuit board (col. 2, lines 12-17 and Fig. 1 item 11). It being understood

that the placement of a connector, which could include the central portion of the circuit board, is placed to optimize connection with the system data and clock signals input lines.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Ode taken with Kawamoto et al. the feature as taught by Chiba et al. in order to provide a PCB with a connector mounted in the central portion of the circuit board that lends a degree of uniformity to the line lengths of the transmission lines mounted on the board, yielding a uniform time duration of signal transmitted from the said connector to the system logic circuits.

6. Claims 9 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ode et al. taken with Kawamoto et al. as applied to claim 1 in item 3 hereinabove, and further in view of Chiba et al..

Relative to claims 9 and 16, Ode et al. taken with Kawamoto et al. **does not teach** a connector for inputting the display data and the clock signal from the display control device being provided in a portion other than a lengthwise end portion of the circuit board.

Ode et al. taken with Kawamoto et al. teaches a video signal line driving circuit of a LCD for the purpose of enabling multilevel gradation display wherein signal lines are divided to accommodate the distribution of signals that have multiple applications in the same system.

Chiba et al. **teaches** a display device (col. 3, lines 16-67; col. 4, lines 1-67 and col. 5, lines 1-36); Chiba et al. further **teaches** a connector for inputting the display data and the clock signal from the display control device being provided in a portion other than a lengthwise end portion of the circuit board (col. 2, lines 12-17 and Fig. 1, item 11).

It would have been obvious to a person of ordinary skill in the art at the time of the invention that the placement of the circuit board connector could be placed other than in a lengthwise end portion of the circuit board; or, in a lengthwise central portion of the circuit board which ever configuration would optimize the signal flow to the bus lines, and/or the placement of the connector relative the mating connection.

It would have further been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Ode et al. taken with Kawamoto et al. the feature as taught by Chiba et al in order to put in place the means to transmit the display data and the clock signals from the display control device to the display device.

7. Regarding claims 10 and 17, the reasons applied to claim 7 in item 4 hereinabove are applicable to claims 10 and 17 as well.

8. Claims 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ode et al. taken with Kawamoto et al. as applied to claim 1 in item 3 hereinabove, and further in view of Hamilton et al.

Regarding claims 11, 12 and 15 Ode et al. further **teaches** the display control device supplies the display data and clock signals to each of the divided bus lines and clock signal lines in sequence in accordance with transmission timing (pg. 3, para. 0063).

Ode et al. taken with Kawamoto et al. **does not teach** said display control device supplies a signal of fixed voltage level to each of the divided bus lines and clock signal lines to which the display data and clock signal lines are not supplied.

Ode et al. taken with Kawamoto et al. teaches a video signal line driving circuit of a LCD for the purpose of enabling multilevel gradation display wherein signal lines are divided to accommodate the distribution of signals that have multiple applications in the same system.

Hamilton et al. **teaches** a control circuit generating a fixed voltage for application to system bus lines wherein a fixed voltage is supplied to a bus line when a data/clock signal is not supplied (col. 29, lines 28-44). It being understood that the system bus lines are brought to a fixed voltage state independent of whether the signal transmission lines are for transmitting date or clock signal.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Ode et al. taken with Kawamoto et al. the feature as taught by Hamilton et al. in order to provide the voltage signals to stabilize the bus lines when data is not being transmitted.

Relative to claims 13-14, Hamilton further **teaches** a control circuit initiating a fixed voltage for application to a signal transmission line (col. 29, lines 28-44).

In a display device, the practice of supplying signals of one voltage to one line of a display matrix while supplying a different voltage to other data or signal lines in the matrix is a common feature of display devices.

Because this practice is common and well know in the art, it would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Ode et al. taken with Kawamoto et al. the feature as taught by Hamilton of generating a fixed voltage for application to the date of clock signal lines of the system.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Ode et al. taken with Kawamoto et al. the feature as taught by Hamilton et al. in order to eliminate the condition whereby the voltage on the signal transmission line/s would be left floating if a fixed voltage were not established.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No.	6,518,946	Ode et al.
U. S. Patent No.	6,166,725	Isami et al.
U. S. Patent No.	6,023,310	Kawamoto et al.
U. S. Patent No.	4,492,460	Considine

Responses

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E Kovalick whose telephone number is 703 306-3020. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703 305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent E. Kovalick
June 7, 2004

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